CLAIMS

What is claimed is:

1. A system for detecting errors in a memory device, the system comprising:

a memory sub-system comprising:

a plurality of memory cartridges configured to store data words;

a cleansing device configured to periodically initiate an internal READ command to the plurality of memory cartridges in response to an event, the internal READ command being issued to the plurality of memory cartridges on a memory network bus; and

a monitoring device configured to monitor the memory network bus and further configured to change the frequency of periodic initiations of the internal READ commands based on the number of requests on the memory network bus over a period of time; and

a host controller operably coupled to the memory sub-system and comprising error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges.

Dub A1

2. The system for detecting errors in a memory device, as set forth in claim 1, wherein each of the plurality of memory cartridges comprises a plurality of memory modules.

3. The system for detecting errors in a memory device, as set forth in claim 2, wherein each of the plurality of memory modules comprises a Dual Inline Memory Module (DIMM).

4. The system for detecting errors in a memory device, as set forth in claim 2, wherein each of the plurality of memory modules comprises a plurality of memory devices configured to store data words.

5. The system for detecting errors in a memory device, as set forth in claim 4, wherein each of the plurality of memory devices comprises a Synchronous Dynamic Random Access Memory (SDRAM) device.

6. The system for detecting errors in a memory device, as set forth in claim 1, wherein the memory sub-system comprises five memory modules.

7. The system for detecting errors in a memory device, as set forth in claim 1, wherein each of the plurality of memory cartridges comprises a memory control device configured to control access to one of the plurality of memory cartridges.

8. The system for detecting errors in a memory device, as set forth in claim 7, wherein each of the memory control devices comprises error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges.

9. The system for detecting errors in a memory device, as set forth in claim 1, wherein the memory controller comprises error detection logic configured to detect errors in a data word during a READ operation.

10. The system for detecting errors in a memory device, as set forth in claim 1, wherein the event comprises an operator instruction.

11. The system for detecting errors in a memory device, as set forth in claim 1, wherein the event comprises the expiration of a timer.

12. The system for detecting errors in a memory device, as set forth in claim 1, wherein the error detection logic comprises Error Code Correction (ECC) logic.

13. The system for detecting errors in a memory device, as set forth in claim 1, wherein the host controller comprises an arbiter configured to schedule accesses to the memory sub-system.

14. The system for detecting errors in a memory device, as set forth in claim 14, wherein the cleansing device is configured to request an internal READ command in the arbiter.

15. The system for detecting errors in a memory device, as set forth in claim 14, wherein the monitoring device is coupled to the cleansing device.

16. The system for detecting errors in a memory device, as set forth in claim 14, wherein the monitoring device is coupled to the arbiter.

17. The system for detecting errors in a memory device, as set forth in claim 16, wherein the monitoring device comprises a plurality of counters configured to count the number of requests are issued to the arbiter.

18. The system for detecting errors in a memory device, as set forth in claim 17, wherein the monitoring device comprises a plurality of timers configured to provide a discrete time period over which the plurality of counters count the number of requests to the arbiter.

19. The system for detecting errors in a memory device, as set forth in claim 18, wherein the number of requests to the arbiter are changed in response to the number of requests counted by the plurality of counters.

20. The system for detecting errors in a memory device, as set forth in claim 19, wherein the requests comprise memory cleansing requests.

21. A memory sub-system comprising:

a plurality of memory cartridges configured to store data words;

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a cleansing device configured to periodically initiate an internal READ command to the plurality of memory cartridges in response to an event, the internal READ command being issued to the plurality of memory cartridges on a memory network bus; and

a monitoring device configured to monitor the memory network bus and further configured to change the frequency of periodic initiations of the internal READ commands based on the number of requests on the memory network bus over a period of time.

22. The memory sub-system, as set forth in claim 21, wherein each of the plurality of memory cartridges comprises a plurality of memory modules.

23. The memory sub-system, as set forth in claim 22, wherein each of the plurality of memory modules comprises a Dual Inline Memory Module (DIMM).

24. The memory sub-system, as set forth in claim 22, wherein each of the plurality of memory modules comprises a plurality of memory devices configured to store data words.

25. The memory sub-system, as set forth in claim 24, wherein each of the plurality of memory devices comprises a Synchronous Dynamic Random Access Memory (SDRAM) device.

26. The memory sub-system, as set forth in claim 21, wherein the memory sub-system comprises five memory modules.

27. The memory sub-system, as set forth in claim 21, wherein each of the plurality of memory cartridges comprises a memory control device configured to control access to one of the plurality of memory cartridges.

28. The memory sub-system, as set forth in claim 27, wherein each of the memory control devices comprises error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges.

29. The memory sub-system, as set forth in claim 21, wherein the memory controller comprises error detection logic configured to detect errors in a data word during a READ operation.

30. The memory sub-system, as set forth in claim 21, wherein the event comprises an operator instruction.

31. The memory sub-system, as set forth in claim 21, wherein the event comprises the expiration of a timer.

32. The memory sub-system, as set forth in claim 21, wherein the cleansing device is configured to request an internal READ command to an arbiter, the arbiter configured to schedule accesses to the memory sub-system.

33. The memory sub-system, as set forth in claim 21, wherein the monitoring device is coupled to the cleansing device.

34. The memory sub-system, as set forth in claim 32, wherein the monitoring device is coupled to the arbiter.

35. The memory sub-system, as set forth in claim 34, wherein the monitoring device comprises a plurality of counters configured to count the number of requests are issued to the arbiter.

36. The memory sub-system, as set forth in claim 35, wherein the monitoring device comprises a plurality of timers configured to provide a discrete time period over which the plurality of counters count the number of requests to the arbiter.

37. The memory sub-system, as set forth in claim 36, wherein the number of requests to the arbiter are changed in response to the number of requests counted by the plurality of counters.

38. The memory sub-system, as set forth in claim 37, wherein the requests comprise memory cleansing requests.

39. A system for correcting errors detected in a memory device, the system comprising:

a memory sub-system comprising:

Sub A1

a plurality of memory cartridges configured to store data words;

a cleansing device configured to periodically initiate an internal READ command to the plurality of memory cartridges in response to an event, the internal READ command being issued to the plurality of memory cartridges on a memory network bus; and

a monitoring device configured to monitor the memory network bus and further configured to change the frequency of periodic initiations of the internal READ commands based on the number of requests on the memory network bus over a period of time; and

a host controller operably coupled to the memory sub-system and comprising:

an arbiter configured to schedule accesses to the memory sub-system;

error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges;

a memory engine configured to correct the errors detected in the data word which has been read from the plurality of memory cartridges in response to the internal READ command initiated by the device and configured to

produce a corrected data word corresponding to the data word in which an error has been detected;

scrubbing control logic configured to request a write-back to each memory location in which the error detection logic has detected an error in a data word which has been read from the memory sub-system; and

one or more memory buffers configured to store the corrected data word.

40. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein each of the plurality of memory cartridges comprises a plurality of memory modules.

41. The system for correcting errors detected in a memory device, as set forth in claim 40, wherein each of the plurality of memory modules comprises a Dual Inline Memory Module (DIMM).

42. The system for correcting errors detected in a memory device, as set forth in claim 40, wherein each of the plurality of memory modules comprises a plurality of memory devices configured to store data words.

43. The system for correcting errors detected in a memory device, as set forth in claim 38, wherein each of the plurality of memory devices comprises a Synchronous Dynamic Random Access Memory (SDRAM) device.

44. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the memory sub-system comprises five memory modules.

45. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein each of the plurality of memory cartridges comprises a memory control device configured to control access to one of the plurality of memory cartridges.

46. The system for correcting errors detected in a memory device, as set forth in claim 45, wherein each of the memory control devices comprises error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges.

47. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the memory controller comprises error detection logic configured to detect errors in a data word during a READ operation.

48. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the event comprises an operator instruction.

49. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the event comprises the expiration of a timer.

50. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the cleansing device is configured to request an internal READ command in the arbiter.

51. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the error detection logic comprises Error Code Correction (ECC) logic.

52. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the host controller comprises an arbiter configured to schedule accesses to the memory sub-system.

53. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the memory engine comprises a Redundant Array of Industry Standard Dynamic Integrated Memory Modules (RAID) memory engine configure to detect and correct failures in a memory device.

54. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the host controller comprises one or more logic devices configured to deliver a scrub request to the arbiter.

55. The system for correcting errors detected in a memory device, as set forth in claim 54, wherein the arbiter is configured to schedule a scrub of the address location corresponding to the data word in which an error is detected.

56. The system for correcting errors detected in a memory device, as set forth in claim 55, comprising a Content Addressable Memory (CAM) controller configured to compare outstanding WRITE requests in the queue of the arbiter with outstanding scrub requests in the queue of the arbiter.

57. The system for correcting errors detected in a memory device, as set forth in claim 56, wherein the scrub request is canceled if an address location of a scrub request contained in the queue is the same as the address location of one of the WRITE requests scheduled prior to the scrub request in the queue.

58. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the cleansing device is configured to request an internal READ command the arbiter.

59. The system for correcting errors detected in a memory device, as set forth in claim 39, wherein the monitoring device is coupled to the cleansing device.

60. The system for correcting errors detected in a memory device, as set forth in claim 58, wherein the monitoring device is coupled to the arbiter.

61. The system for correcting errors detected in a memory device, as set forth in claim 58, wherein the monitoring device is coupled to the scrubbing control logic.

62. The system for correcting errors detected in a memory device, as set forth in claim 61, wherein the monitoring device comprises a plurality of counters configured to count the number of requests are issued to the arbiter.

63. The system for correcting errors detected in a memory device, as set forth in claim 62, wherein the monitoring device comprises a plurality of timers configured to provide a discrete time period over which the plurality of counters count the number of requests to the arbiter.

64. The system for correcting errors detected in a memory device, as set forth in claim 63, wherein the number of requests to the arbiter are changed in response to the number of requests counted by the plurality of counters.

65. The system for correcting errors detected in a memory device, as set forth in claim 64, wherein the requests comprise memory cleansing requests.

66. The system for correcting errors detected in a memory device, as set forth in claim 64, wherein the requests comprise memory scrub requests.

67. A method for dynamically scheduling access to a memory sub-system, comprising the acts of:

(a) monitoring activity on a memory bus configured to provide access to the memory sub-system; and

(b) periodically initiating internal READ commands from a cleansing device in the memory sub-system, wherein the period between initiating each READ command is dependent on the activity on the memory bus.

68. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 67, wherein the activity comprises a plurality of memory requests.

69. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 68, wherein the act of monitoring activity on the memory bus is performed by a Memory Bus Utilization Monitor (MBUM).

70. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 69, wherein the MBUM comprises a plurality of counters configured to count the number of requests on the memory bus over a length of time.

71. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 70, wherein the MBUM comprises a plurality timers coupled to the plurality of counters and configured to set the length of time over which the plurality of counters are configured to count the number of requests on the memory bus.

72. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 71, wherein the number of requests determined by the plurality of counters over the length of time set by the plurality of timers, is compared to a threshold.

73. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 72, wherein the period between initiating each READ command is increased if the number of requests determined by the plurality of counters is greater than the threshold.

74. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 72, wherein the period between initiating each READ command is decreased if the number of requests determined by the plurality of counters is less than the threshold.

75. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 67, wherein the internal READ command is a cleansing operation request.

76. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 67, further comprising the acts of:

transmitting a first set of data corresponding to the address issued in the internal READ command, from the memory sub-system to a host-controller;

detecting errors in the first set of data; and

producing a second set of data from the fist set of data, wherein the second set of data comprises corrected data and corresponds to the address in the first set of data.

77. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 76, comprising the acts of:

storing the second set of data and corresponding address in a temporary storage device;

scheduling a scrub of the address corresponding to the second set of data; and

writing the second set of data to the corresponding address location to replace the first set of data in the memory sub-system.

78. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 77, wherein the memory sub-system comprises a plurality of memory cartridges.

79. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 78, wherein each of the plurality of memory cartridges comprises a plurality of memory modules.

DUB A1

80. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 79, wherein each of the plurality of memory modules comprises a plurality of memory devices configured to store data words.

81. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 80, wherein each of the plurality of memory cartridges comprises a corresponding memory control device.

82. The method for dynamically scheduling access to a memory sub-system, as set forth in claim 81, wherein the memory controller comprises a plurality of memory control devices, each of the plurality of memory control devices corresponding to one of the plurality of memory cartridges.

83. The method for correcting errors detected in a memory sub-system, as set forth in claim 76, wherein act (b) comprises the act of using ECC methods to detect errors in the set of data.

84. The method for correcting errors detected in a memory sub-system, as set forth in claim 76, wherein act (c) comprises the act of correcting the errors detected in the first set of data

using a Redundant Array of Industry Standard Dual Inline Memory Modules (RAID) memory engine configured to detect and correct failures in a memory device.

85. The method for correcting errors detected in a memory sub-system, as set forth in claim 84, wherein the second set of data is produced by the RAID memory engine.